Q.P. Code: 16CS506 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Supplementary Examinations December-2021

DIGITAL LOGIC DESIGN

(Common to CSE & CSIT)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Convert the following numbers i)$(41.6875)_{10}$ to Hexadecimal number ii)$(11001101.0101)_2$ to base-8 and base-4 iii)$(4567)_{10}$ to base2	L5	6M
	b	Subtract $(111001)_2$ from (101011) using 1's complement?	L5	6M
		OR		
2	a	Convert the following numbers i) $(AB)_{16}$ = ( )$_2$ ii)) $(1234)_8$ = ( )$_{16}$ iii)$(101110.01)_2$=( )$_8$	L5	6M
	b	Perform the following Using BCD arithmetic $(7129)_{10} + (7711)_{10}$	L5	6M
		UNIT-II		
3	a	Simplify the following Boolean expression using K-MAP and implement using NAND gates F(W,X,Y,Z) = XYZ+WXY+WYZ+WXZ.	L5	6M
	b	Simplify the Boolean expression using K-MAP F(A,B,C,D) = $\sum$m(1,2,3,8,9,10,11,14)+d(7,15).	L5	6M
		OR		
4	a	Simplify the Boolean expression using K-map. F(A,B,C,D,E)= $\sum$m(0,1,4,5,16,17,21,25,29)	L5	6M
	b	Obtain the minimal product of sums and design using NAND gates F(A,B,C,D)= = $\sum$m(0,2,3,6,7) +d(8,10,11,15)	L5	6M
		UNIT-III		
5	a	Explain about parallel Adder.	L2	6M
	b	Explain Design Procedure of combinational circuits.	L2	6M
		OR		
6	a	Design the combinational circuit binary to gray code.	L5	6M
	b	Explain about Binary Half Adder.	L2	6M
		UNIT-IV		
7	a	Explain the Logic diagram of SR flip-flop.	L2	6M
	b	Design and draw the 3 bit up-down synchronous counter.	L5	6M
		OR		
8	a	Draw and explain the operation of D Flip-Flop.	L5	6M
	b	Explain about Shift Registers.	L2	6M
		UNIT-V		
9	a	Encode the 11-bit code 10111011101 into 15 bit information code.	L3	6M
	b	Explain the memory decodir g error detection and correction.	L2	6M
		OR		
10	a	Explain about the construction of 4 X 4 RAM.	L2	6M
	b	Explain different types of ROM.	L2	6M

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